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PATENT APPLICATION
DOCKET NO.: 200210141-2

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the pending claims.

1. (Original) A method for providing reset control between two integrated circuit domains (ICDs) disposed in a synchronous relationship, comprising:

generating control signals in a first ICD for resetting driver circuitry therein in a phased manner, said driver circuitry for driving a signal towards a second ICD on a signal path;

generating an inter-ICD reset control signal in said first ICD for transmission to said second ICD; and

resetting driver circuitry in said second ICD upon receiving said inter-ICD reset control signal from said first ICD.

2. (Currently Amended) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 1, wherein said driver circuitry in said first ICD is reset in a phased manner by providing first and second control signals, wherein said driver circuitry drives said signal towards said second ICD only after said first and second control signals have been asserted ~~are generated in said first ICD responsive to a reset.~~

3. (Original) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 1, wherein said driver circuitry in said first ICD is reset in a phased manner by providing two control signals thereto, a first control signal operating to release said driver circuitry from a tristated condition and a second control signal operating to toggle said driver circuitry for driving appropriate logic levels with respect to said signal towards said second ICD.

4. (Original) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 3, wherein said driver circuitry in said first ICD is operable to drive a strobe signal towards said second ICD.

5. (Original) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 3, wherein said driver circuitry in said first ICD is operable to drive a data signal towards said second ICD.

6. (Original) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 3, wherein said first control signal is generated based on a system reset signal.

7. (Original) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 6, wherein said second control signal is generated by a reset control block disposed in said first ICD, said reset control block operating responsive to a power reset signal.

8. (Original) The method for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 1, wherein said second ICD includes clock distribution circuitry for manufacturing a local clock signal based on a transported clock signal provided by said first ICD.

9. (Original) A system for providing reset control between two integrated circuit domains (ICDs) disposed in a synchronous relationship, comprising:

circuitry that produces control signals in a first ICD to reset driver circuitry therein in a phased manner, said driver circuitry driving a signal towards a second ICD on a signal path; and

circuitry that produces an inter-ICD reset control signal in said first ICD that is transmitted to said second ICD, said inter-ICD reset control signal operating to reset driver circuitry in said second ICD.

10. (Currently Amended) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 9, wherein said driver circuitry in said first ICD is reset in a phased manner by providing first and second control signals, wherein said driver circuitry drives said signal towards said second ICD only after said first and second control signals have been asserted ~~are generated in said first ICD responsive to a reset.~~

11. (Original) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 9, wherein said driver circuitry in said first ICD is reset in a phased manner by providing two control signals thereto, a first control signal operating to release said driver circuitry from a tristated condition and a second control signal operating to toggle said driver circuitry for driving appropriate logic levels with respect to said signal towards said second ICD.

12. (Original) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 11, wherein said driver circuitry in said first ICD is operable to drive a strobe signal towards said second ICD.

13. (Original) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 11, wherein said driver circuitry in said first ICD is operable to drive a data signal towards said second ICD.

14. (Original) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 11, wherein said first control signal is generated based on a system reset signal.

15. (Original) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 14, wherein said second control signal is generated responsive to a power reset signal.

16. (Original) The system for providing reset control between two ICDs disposed in a synchronous relationship as set forth in claim 9, wherein said second ICD includes clock distribution circuitry for manufacturing a local clock signal based on a transported clock signal provided by said first ICD.

17. (Original) A computer system having at least two integrated circuit domains (ICDs) disposed therein in a synchronous communication relationship, comprising:

means for generating control signals in a first ICD for resetting driver circuitry therein in a phased manner, said driver circuitry for driving a signal towards a second ICD on a signal path; and

means for generating an inter-ICD reset control signal in said first ICD for transmission to said second ICD, said inter-ICD reset control signal operating to reset driver circuitry in said second ICD.

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18. (Original) The computer system as set forth in claim 17, wherein said driver circuitry in said first ICD is reset in a phased manner by providing two control signals thereto, a first control signal operating to release said driver circuitry from a tristated condition and a second control signal operating to toggle said driver circuitry for driving appropriate logic levels with respect to said signal towards said second ICD.

19. (Original) The computer system as set forth in claim 18, wherein said driver circuitry in said first ICD is operable to drive a strobe signal towards said second ICD.

20. (Original) The computer system as set forth in claim 18, wherein said driver circuitry in said first ICD is operable to drive a data signal towards said second ICD.

21. (Original) The computer system as set forth in claim 18, wherein said first control signal is generated based on a system reset signal.

22. (Original) The computer system as set forth in claim 21, wherein said second control signal is generated responsive to a power reset signal.

23. (Original) The computer system as set forth in claim 17, wherein said second ICD includes clock distribution circuitry for manufacturing a local clock signal based on a transported clock signal provided by said first ICD.

24. (Original) The computer system as set forth in claim 23, wherein said local clock signal in said second ICD is operable to activate a strobe generation block disposed therein for generating a strobe signal towards said first ICD.